

# **An Approximate Timing Analysis Framework for Complex Real-Time Embedded Systems**

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## **Abstract**

To maintain, analyze and reuse many of today's Complex Real-Time Embedded Systems (CRTES) is very difficult and expensive, which, nevertheless, offers high business value concerning great concern in industry. In such context, both functional and non-functional behavior of systems have to be assured, e.g., Worst-Case Response Time (WCRT) of tasks has to be known. However, due to high complexity of such systems and the nature of the problem, the exact WCRT of tasks is impossible to find in practice, but can only be bounded. In this thesis, we address this challenge by presenting a simulation framework for approximate timing analysis of CRTES, namely AESIR-CORES, which uses three novel contributions. Our evaluation using three models inspired by two fictive but representative industrial CRTES indicates that AESIR-CORES can either successfully obtain the actual WCRT values, or have the potential to bound the unknown actual WCRT values from a statistical perspective.